Algorithms and Framework for Energy Efficient Parallel Stream Computing on Many-Core Architectures

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Outline

High performance computing

Constant struggle for performance

High performance computing

Constant struggle for performance: Hollerith census machine

- Census every 10 years.

Picture: "HollerithMachine.CHM" by Adam Schuster

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High performance computing

Constant struggle for performance: Hollerith census machine

- Census every 10 years.
- 8 years in 1880.

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High performance computing

Constant struggle for performance: Hollerith census machine

- Census every 10 years.
- 8 years in 1880.
- 1 year in 1890.

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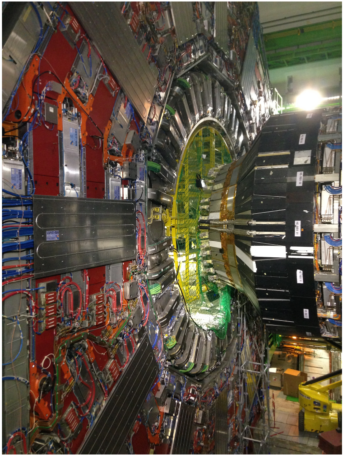
High performance computing

Constant struggle for performance: Big data.

- Social medias
- Internet of things



High performance computing

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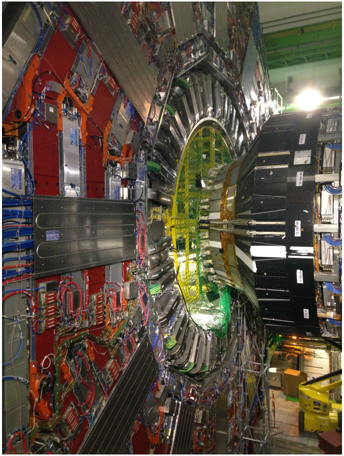
Applications:

- Scientific computing



Picture: “View inside detector at the CMS cavern LHC CERN” by Tighef

High performance computing

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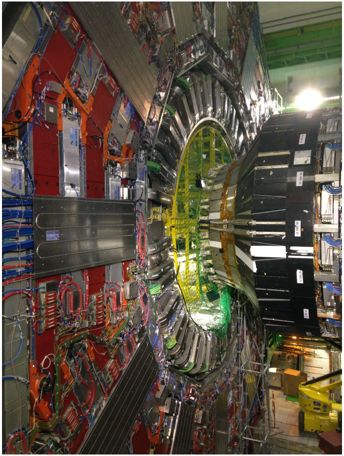

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Applications:

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- Marketing

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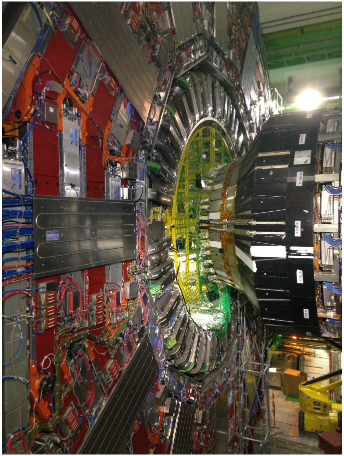

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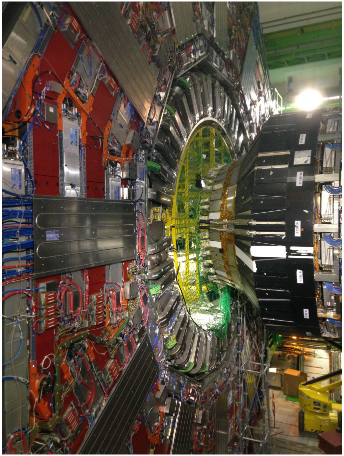
- Intelligence (GCHQ)



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Accelerate computation

How to improve performance?

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- Miniaturize
    - End of Moore's law?

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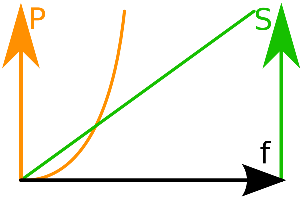
  - Too high energy consumption



Accelerate computation

How to improve performance?

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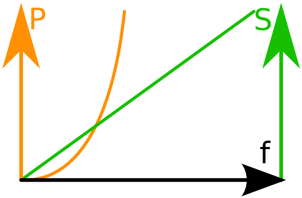

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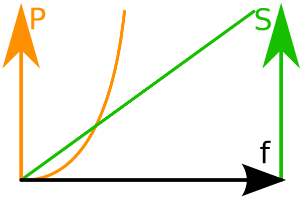

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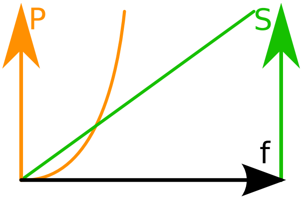
  - Better energy consumption
  - Very challenging
    - Instruction-Level parallelism Wall



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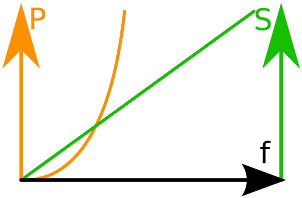
    - Scalability issues for consistent shared memory



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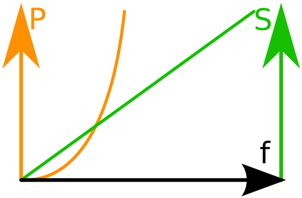
    - Scalability issues for consistent shared memory
    - Von-Neumann bottleneck



Streaming computation

Streaming

- Software pipelining
- Tasks execute in parallel in steady-state

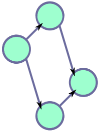


Figure: Streaming taskgraph.

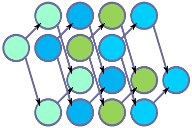


Figure: Pipelined execution of streaming taskgraph.

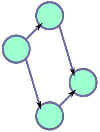
Streaming computation

Streaming

- Software pipelining
- Tasks execute in parallel in steady-state

Static scheduling

- Moldable tasks
- Steady state
- Throughput constraint
- Optimize energy



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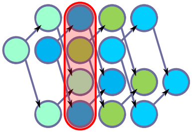

Figure: Steady state of the streaming pipeline.

Streaming computation

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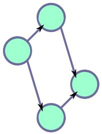
Streaming Task Collection

- Independent tasks
- Balance workload
- No communication cost



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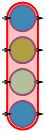


Figure: Independent tasks in the steady state.

Platform model

Platform

- *p* uniform processors
- Discrete frequency set *F*
  - Applied to individual cores
  - Voltage by auto-co-scaling
  - Can change dynamically any time

Power model

- Dynamic power function of frequency
  - Analytic function or measurements
  - No restriction
  - Replaceable
- Energy linear in time, power and number of processors running

Task model

Moldable task j

- Fixed work τ_j
- Allocation: run on $w_j \geq 1$ cores
  - Maximum W_j: $w_j \leq W_j$
- Arbitrary efficiency function
  - $0 < e_j(q) \leq 1$ for $1 \leq q \leq W_j$
  - No convexity, monotony or continuity constraint
- Time proportional to work, parallel degree and frequency

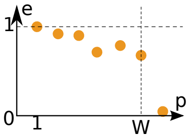


Figure: Arbitrary efficiency function.

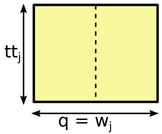
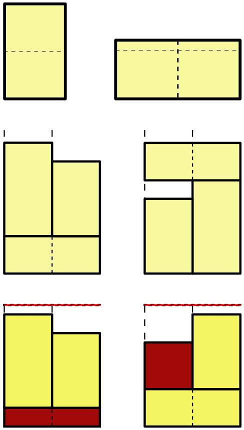


Figure: Moldable task.

Problem formulation

3 static problems

- Resource allocation
  - Find $w_j \leq min(p, W_j)$ for each task j
  - Define execution time of tasks j
- Task mapping to cores
  - Assign tasks to a subset of cores $1..p$
- Discrete frequency scaling
  - Assign tasks a frequency level in F
  - Respect a makespan constraint M
- Repeated execution of a task sequence
- Non data-ready tasks are delayed to the next round



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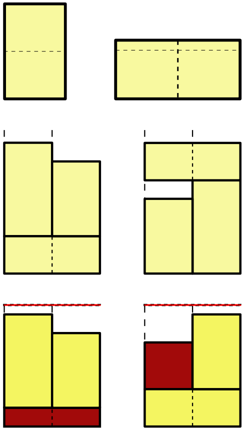
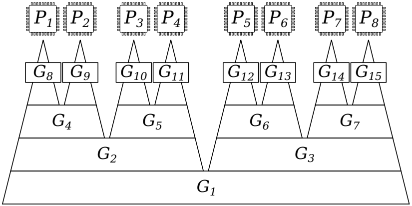
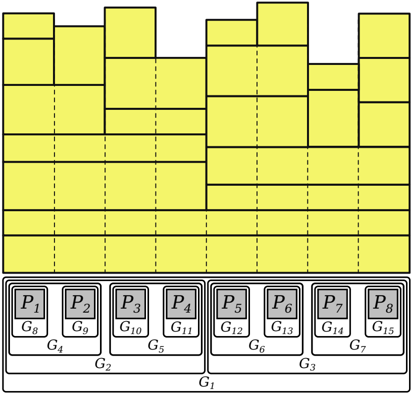
All steps influence each other



Crown scheduling

Restrict allocation and mapping to $O(p)$ processor subsets (groups)





- Tasks must be allocated as many cores as the size of a group
- Reduce possible mapping targets from $2^p - 1$ groups to $2p - 1$

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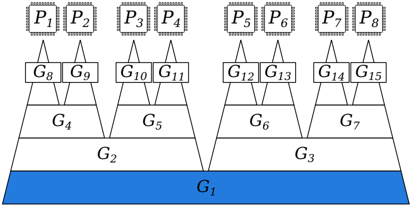

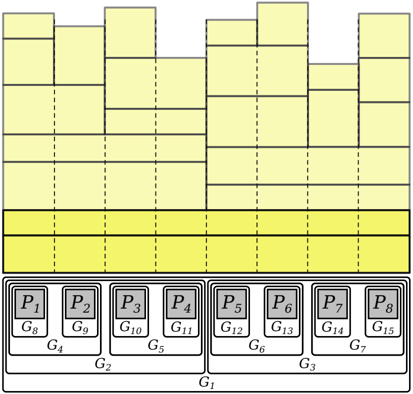

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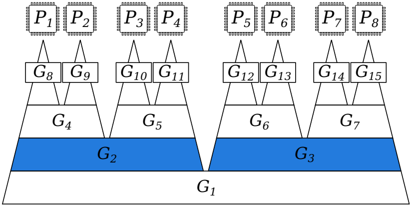

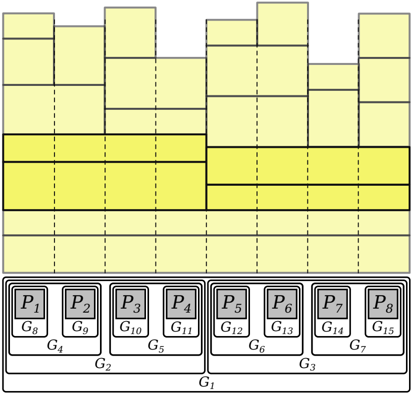

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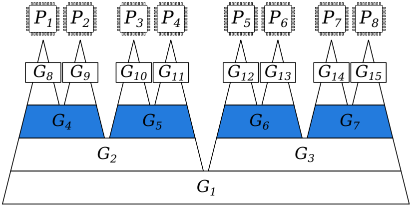

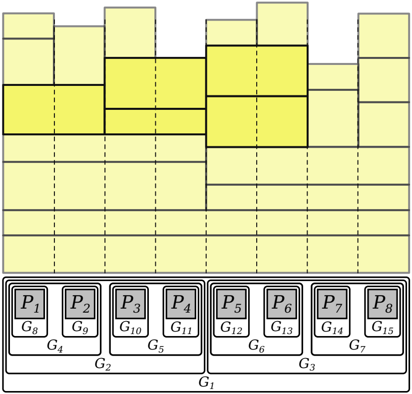

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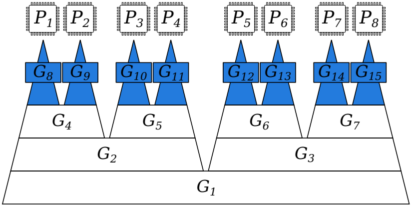

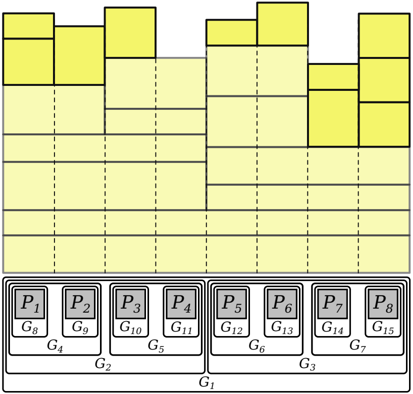

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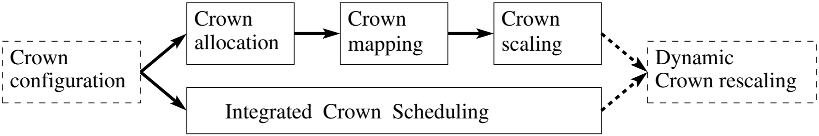
Crown scheduling

Computing a crown schedule

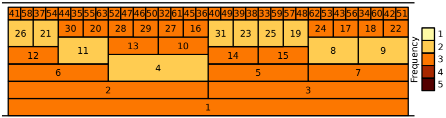
- Separated or integrated phases

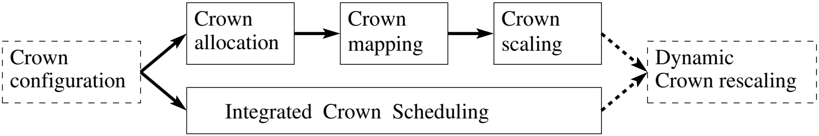


- ILP formulations for each step and for integrated scheduler by (Kessler et al. [2013])
  - Phase separation prevents compromises
  - Phase integrated constrained by the crown structure
  - Slow and limited in input problem size

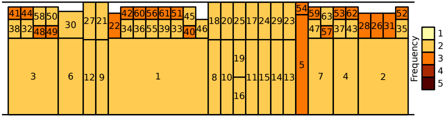
Crown scheduling

Phase-separated





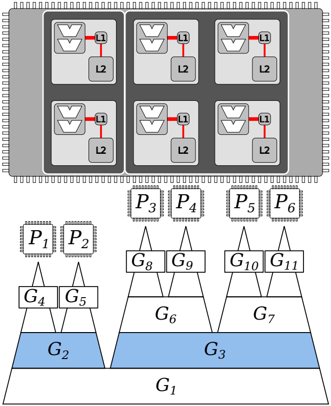
Integrated



Crown Extensions

Adapt to realistic processors

- $p \neq 2^i$
- Constraints: frequency islands



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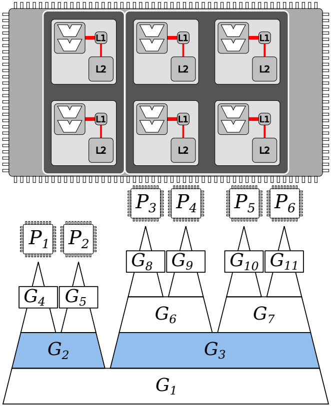
Crown Configuration



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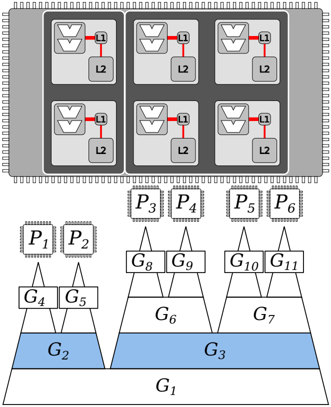
Crown Configuration

Crown Consolidation

- Account for idle energy
- Switch unused cores off



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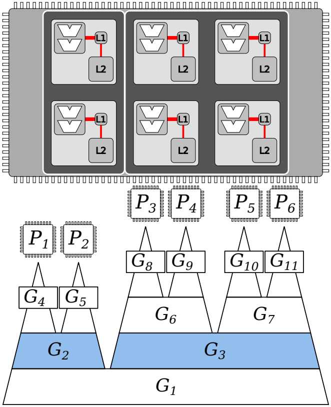
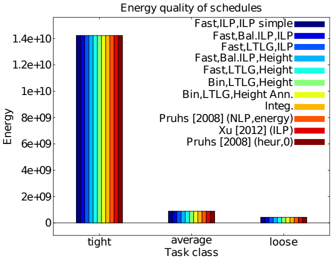
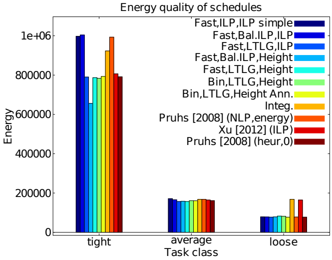
Provable approximation



Voltage Islands topology influence





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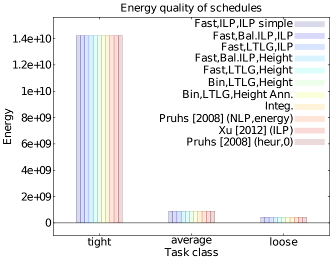

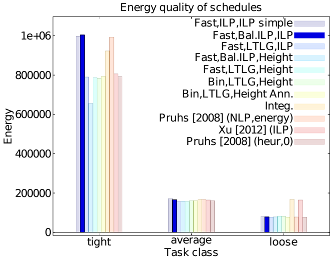

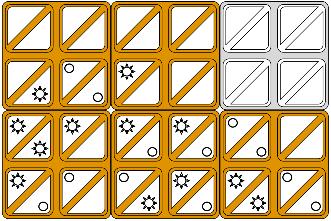

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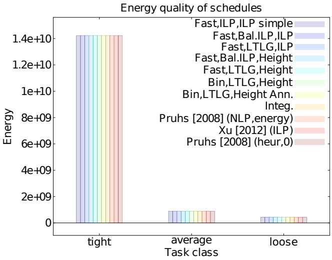

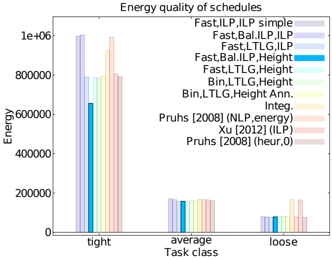

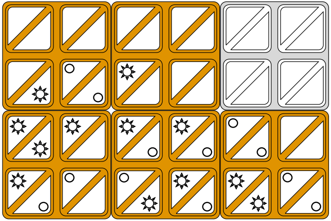

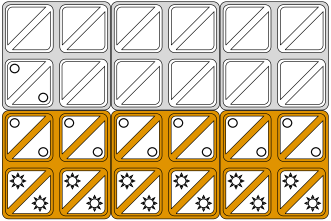

Example: Mergesort

Developed by JohN Von Neumann in 1945 (Knuth [1998])

- *External* algorithm

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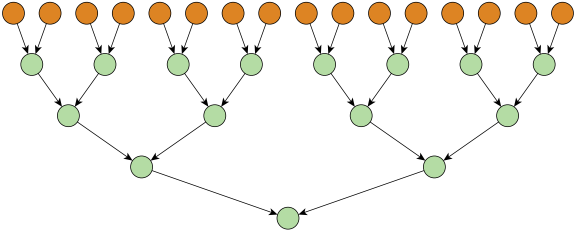
- *External* algorithm
- Limits use of slow memories
- Stream program: tree structure



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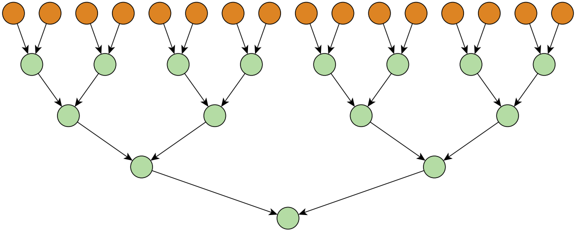
- Stream program: tree structure
  - Leaves: presort (non-streamed)



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- *External* algorithm
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- Stream program: tree structure
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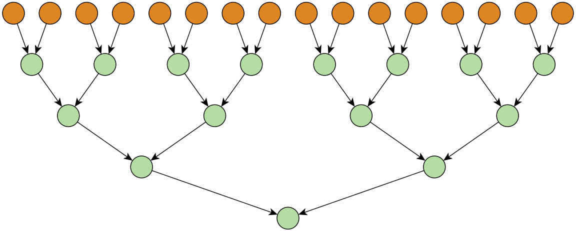
  - other: merge (streamed)



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Developed by JohN Von Neumann in 1945 (Knuth [1998])

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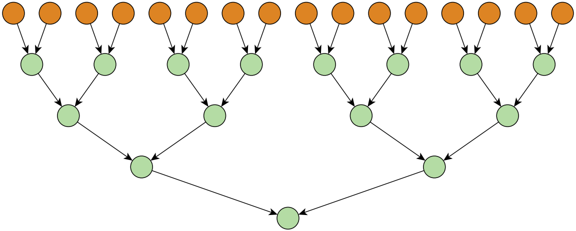

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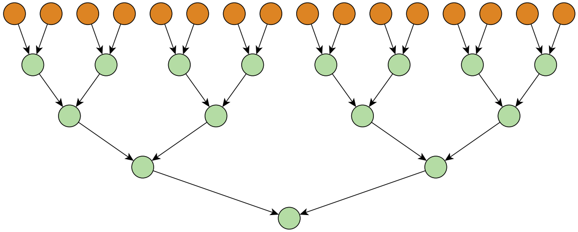

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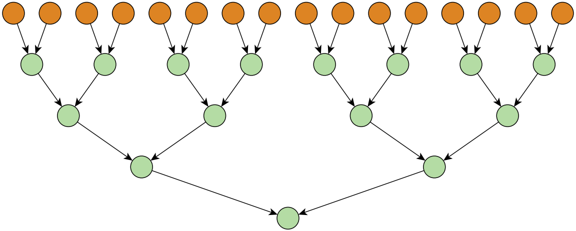
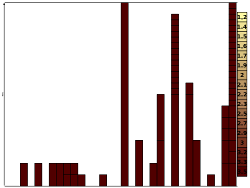


https://www.youtube.com/watch?v=XaqR3G_NVoo

Island-aware scheduling: mergesort

All cores in one island: 100%



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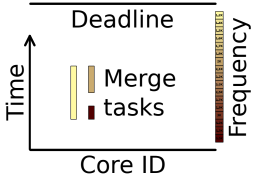

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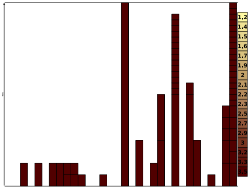

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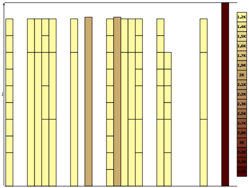

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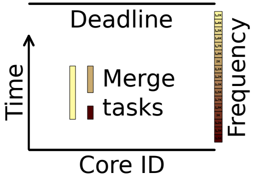

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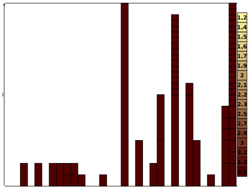

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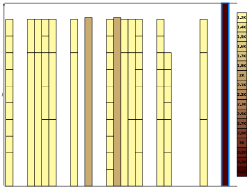

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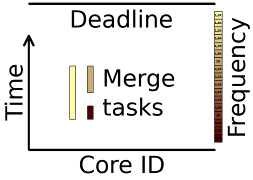

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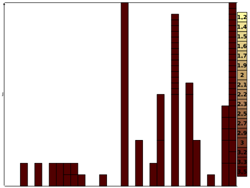

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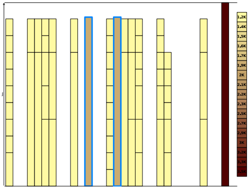

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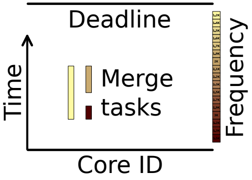

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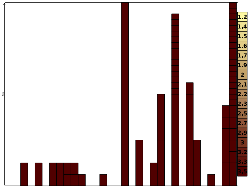

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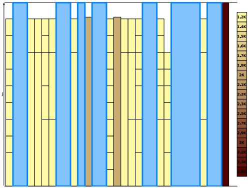

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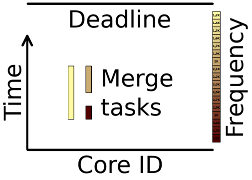

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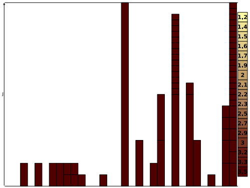

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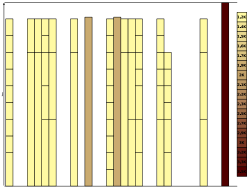

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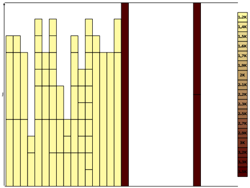

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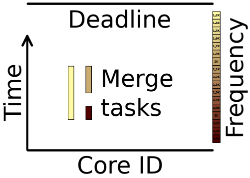

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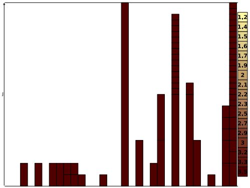

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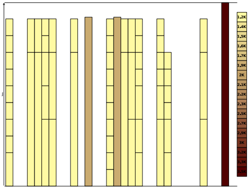

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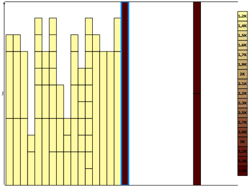

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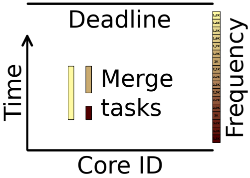

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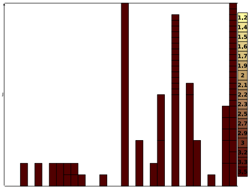

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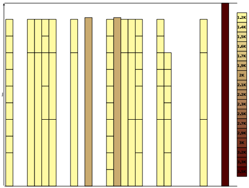

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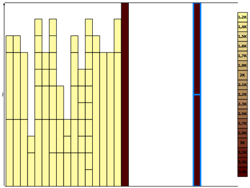

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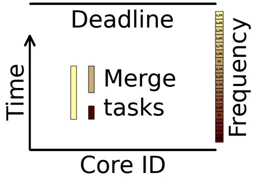

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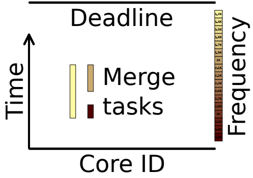

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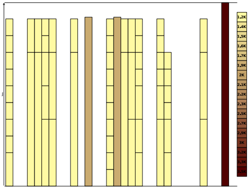

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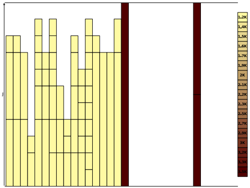

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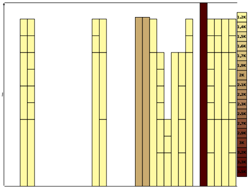

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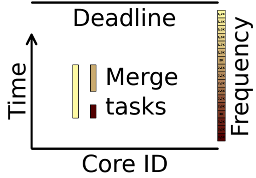

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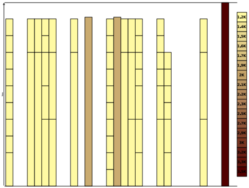

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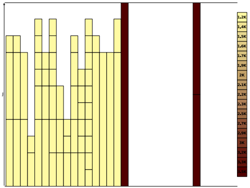

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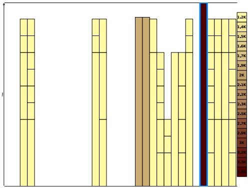

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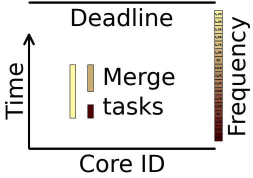

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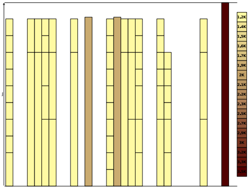

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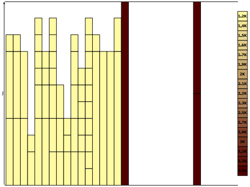

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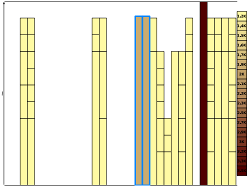

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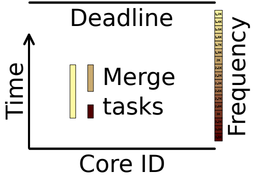

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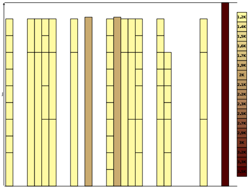

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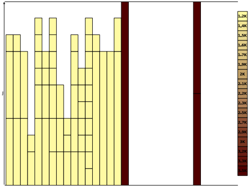

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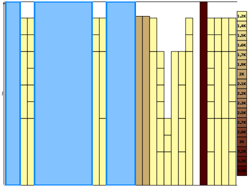

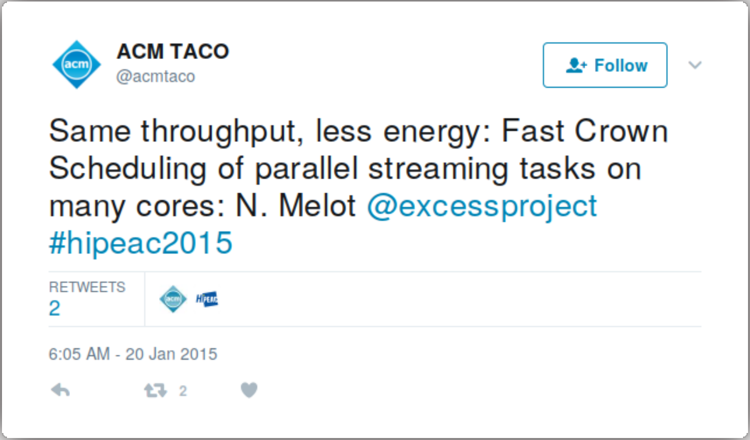
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@acmtaco
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Same throughput, less energy: Fast Crown Scheduling of parallel streaming tasks on many cores: N. Melot @excessproject #hipeac2015
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Drake

Stream programming framework

- On-chip pipelining

Drake

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- Moldable tasks

Drake

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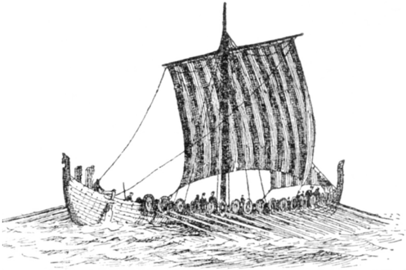

Drake: derived from Schedeval (Janzén [2014])

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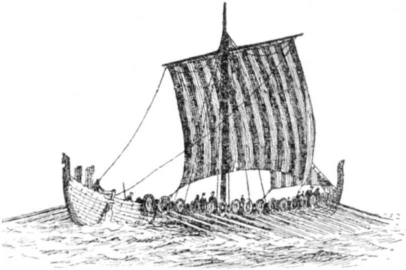

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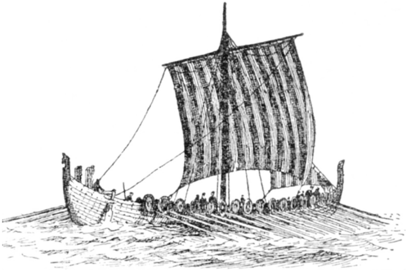

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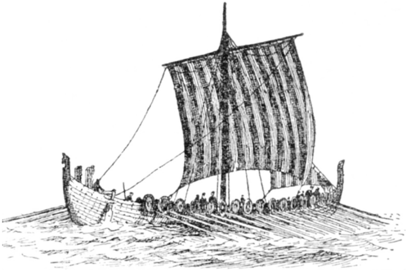

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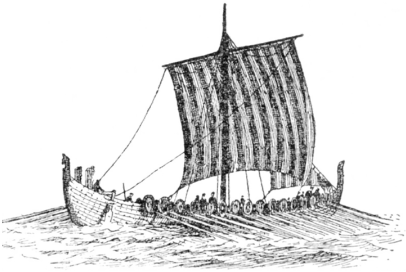

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Takes code to execute on target platform

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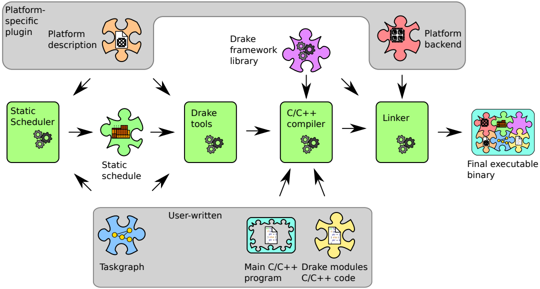

Conclusion

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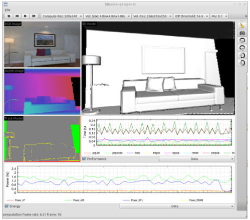
Simultaneous Localization And Mapping



Future work

Investigate more scheduling techniques

- Minimize communication costs
- Heterogeneous platforms
- Quasi-static scheduling
- Schedule main memory accesses
- Port Drake to mores architectures
- Implement Synchronous Data Flow for Drake
- Optimize on-chip memory usage

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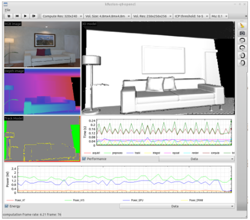

Other applications:

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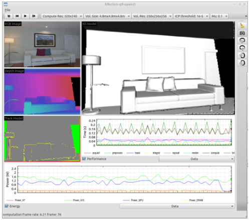

Other applications:

- Machine learning
- Provable High Performance Computing

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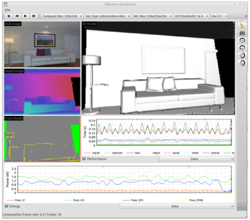

Other applications:

- Machine learning
- Provable High Performance Computing
- Aeronautic

Questions

Thank you for your attention.

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