Genus Numerics Group 2017 Summer Internships

Background

The Genus® Numerics Group focuses on all aspects of mathematical hardware design for Cadence's Genus division. This is a customer facing applied research group comprised of computer arithmetic experts. The Genus synthesis solution is accompanied by an IP library of off-the-shelf components, ChipWare®. These components cover a wealth of mathematical functions. These components must lead the market in terms of hardware quality, power, area & delay. The actively growing numerical ChipWare library drives innovation within the Numerics Group. It provides a unique source of customer facing designs that challenge computer arithmetic architecting, design, optimization, verification and utilisation. The Numerics group also owns the fundamental arithmetic component designs within the Genus synthesis solution and thus provides an opportunity for highly synergistic software and hardware development.

The realisation that deep mathematical and logical reasoning can deliver significant hardware benefits in terms of reliability, speed, area and power efficiency is at the core of the group's formation. From automatic design space exploration through to accuracy analysis, the Numerics group offers and faces a myriad of fascinating challenges. The following paper gives a flavour of the questions we explore http://cas.ee.ic.ac.uk/people/gac1/pubs/TheoISCAS12.pdf.

We grapple with the most challenging questions in the area of mathematical hardware design. Genus's differentiation rests on innovation at all levels of composition and implementation of the fundamental hardware mathematical operations.

Opportunity

As part of the group's growth we are looking to fill two 3 month internship positions for Summer 2017. We are looking to find talented individuals who will share our passion for computer arithmetic. The Numerics Group's position within Cadence provides the opportunity to work with other key divisions. In particular, we have strong links with the Stratus High Level Synthesis (HLS) Division, Jasper Model Checking Division and the Conformal Equivalency Checking Division. Thus our work draws upon formal verification expertise and higher level system. Combined with the broad range of Genus customer and ChipWare library designs, our range of projects and interests is incredibly broad while always being firmly connected to the arithmetic. Our possible internship projects reflect this:

- Advanced HLS - High Level Synthesis of numerically intensive algorithms can be improved by altering hardware parameters, such as precision, while maintaining application level correctness. This project is linked to notions of approximate computing and automated design space exploration (DSE). Background reading: http://www.doc.ic.ac.uk/~tbecker/papers/fccm14mk.pdf
- DSE for ChipWare - Automatic design space exploration for the implementation of ChipWare components, e.g. transcendental functions such as sin(x).
- DSE for Genus – Automatic design space exploration by rewriting arithmetic expressions within Genus. Background reading: http://cas.ee.ic.ac.uk/people/gac1/pubs/XitongFPT13.pdf
- Arithmetic Hardware Scrubbing – Formal verification tools can be used to find arithmetically dead code that is unoptimised by synthesis tools. This approach actually uses verification tools to improve hardware quality rather than simply proving correctness.

- Arithmetic Assertion Based Synthesis – synthesis results can be significantly improved by exploiting known ranges or correlations between input signals. This project explores automatic exploitation of such data assertions.
- ChipWare Innovation – improve or build new Chipware components by inventing novel implementations to the core arithmetic operations. New customer and internal requests provide a constant stream of new and challenging designs.
- Arithmetic Formal Verification – the verification of arithmetic circuits is a significant challenge. A combination of both Jasper and Conformal tools are invariably used during our verification processes. However, arithmetic verification is amenable to unique mathematical approaches whose scalability and applicability is always worth exploring. Background reading: http://cas.ee.ic.ac.uk/people/gac1/pubs/TheoDACKC11.pdf

Interns will have access to the range of Cadence tools and these projects drive their creative and combined use. Our group members are true subject experts and this internship offers a unique insight into their work and various aspects of arithmetic hardware design. The internship serves as a unique insight into the multitudinous fascinating challenges faced by the EDA sector.

Skills

The group draws equally upon electrical engineering, computer science and mathematics. We value defining and answering the fundamental questions - even the most basic questions are a potential source of invention. Working as part of the diverse Genus team we place considerable value on the ability and interest in providing complete, clear and concise delivery of complex material.

Required Skills and Qualifications

- Solid Mathematical Background
- Excellent Creative Analytic Problem Solving Skills
- Meticulous Attention to Detail
- Currently engaging in a Degree, Masters or PhD in Electrical/Electronic Engineering, Computing or Mathematics

Personality - Successful candidates will be/have:

- Highly inquisitive
- A passion for excellence with a flair for detail
- Tenacious in identifying, analyzing & recommending improvements & innovations
- Excellent communicator
- Friendly and patient with high levels of technical empathy

Duration Three month Summer 2017 internship with flexible start date, extensions possible

Location Cadence Cambridge - Byron House, Cambridge Business Park, Cambridge, CB4 0WZ

Applications https://cadence.wd1.myworkdayjobs.com/en-US/External_Careers/job/CAMBRIDGE-02/Genus-Numerics-Group-2017-Summer-Internships_R20195